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(54) Structure and fabrication of high dielectric constant metal/dielectric/semiconductor capacitor for use as a storage capacitor in memory devices.

(57) A capacitor for a semiconductor structure is formed having a substrate (10), a stack of a buffer layer (12) and a layer of ferroelectric material (14), and a top electrode (16). The capacitor can also have a layer of polysilicon (11) between the sub – strate (10) and the buffer layer (12). A method for forming the same, through establishing a substrate (10), a buffer layer (12) and a layer of ferroelectric material (14), defining and annealing the buffer layer and layer of ferroelectric material (14), and estab – lishing a top electrode (16), is also disclosed.

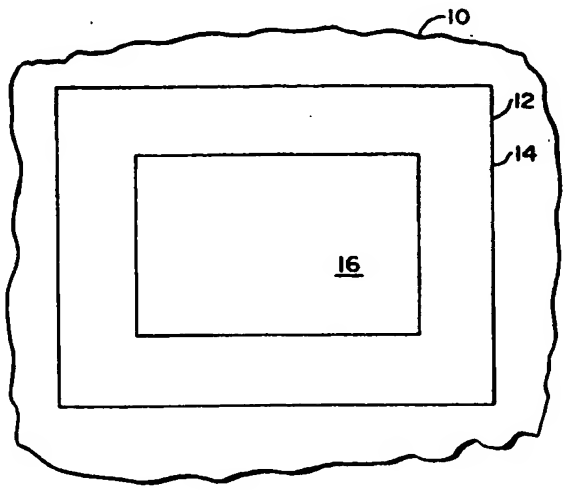

FIG.5

EP 0 540 994 A1

The present invention is directed to a ferroelectric capacitor having a silicon/dielectric/metal structure.

Presently, silicon dioxide is used as the dielectric in the storage capacitor of dynamic random access memory (DRAM) cells. However, as densities increase to the 64 M-bit range and beyond, charge storage using a SiO_2 capacitor requires a large amount of space (area) due to the low dielectric constant of SiO_2, which is approximately 3.9. The large area required by these capacitors results in the capacitor being too large to be of practical use in the industry. As a result, the industry has been in search of a material to replace silicon dioxide as the dielectric in a capacitor. With a larger dielectric constant, assuming the separation between capacitor plates remains the same, the same capacitance is obtained using a smaller area.

One material that has been considered for possible use as the dielectric in a capacitor is a ferroelectric material, such as a compound comprising lead zirconate titanate ("PZT") . Ferroelectric materials are of interest because materials such as PZT have a high dielectric constant. In U.S. Patent No. 4,853,893 to Eaton, Jr. and Parris, owned by Ramtron Corporation of Colorado Springs, Colorado, there is a discussion of using PZT as a dielectric material for a DRAM memory cell capacitor. That citation calls for substituting PZT for SiO_2. Col. 9, line 57 et seq. See also, U.S. Patent No. 4,536,785 to Gibbons.

However, when a ferroelectric material is established on a silicon substrate, interdiffusion occurs between the ferroelectric material and the silicon substrate. As a result, a low dielectric constant layer is formed in series with the ferroelectric material causing the resulting structure (a stack) to appear as two capacitors in series, one with a low dielectric constant and one with a high dielectric constant (the ferroelectric material). This causes the effective dielectric constant of the entire stack to decrease two orders of magnitude. The two order decrease occurs because the existence of the low dielectric constant layer dominates the total capacitance of the entire stack. Accordingly, the result is a capacitor with an average capacitance rather than one with a very high capacitance as would be obtained when using a ferroelectric material without a low dielectric constant layer in series with it.

The use of a high dielectric constant stack comprising a buffer layer, a layer of ferroelectric material and a second buffer layer as the gate dielectric in a field effect transistor is the subject of an invention and companion patent application entitled Structure and Fabrication of High Transconductance MOS Field Effect Transistor Using A Buffer Layer/Ferroelectric/Buffer Layer Stack as the Gate Dielectric by the same inventors as this application, George Argos, Jr. and T. S. Kalkur (attorney docket no. RAM 342) and which is incorporated herein by reference.

The object of the present invention is to provide a capacitor and method of fabrication therefor which does not suffer from the serious drawbacks we have described.

The present invention in one of its aspects is directed to a ferroelectric capacitor for use in memory devices which require charge storage. In particular, the present invention will be useful in products which have limited area requirements, such as high density DRAMs.

The ferroelectric capacitor of the present invention overcomes the previously described problem by having a buffer layer between a substrate and a layer of ferroelectric material. The buffer layer inhibits the interdiffusion between the high dielectric constant, ferroelectric material and the silicon of the substrate. This configuration prevents the formation of a low dielectric constant material in series with the ferroelectric material. A top electrode is located over the ferroelectric material. In another embodiment, a layer of polysilicon (which preferably has been doped for conductivity) acts as a bottom electrode and is located between the substrate and the buffer layer.

The present invention is further directed to a method for forming a ferroelectric capacitor. In general, the method comprises a sequence of deposition and defining steps to form a semiconductor capacitor having a substrate, a buffer layer, a layer of ferroelectric material and a top electrode.

In describing the preferred embodiment, reference is made to the accompanying drawings wherein like parts have like reference numerals, and wherein:

Figure 1 is a cross-sectional view of a portion of a capacitor according to an embodiment of the present invention wherein a buffer layer is located over a substrate;

Figure 2 shows the structure of Figure 1 with a layer of ferroelectric material over the buffer layer; both the buffer layer and the layer of ferroelectric material having been patterned and etched;

Figure 3 shows the structure of Figure 2 with a defined top electrode over the layer of ferroelectric material;

Figure 4 is a cross-sectional view of a capacitor according to another embodiment of the present invention wherein a layer of polysilicon is located between the substrate and the buffer layer; and

Figure 5 is a plan view of a capacitor constructed according to the preferred embodiment.

The method of the present invention comprises a series of fabrication steps which are carried out in the manner set forth below, with the reference to a preferred embodiment of using the method.

In Figure 1, in accordance with a first embodiment of the present invention, a substrate 10 preferably comprises silicon. The substrate can be comprised of, for example, polysilicon, undoped crystal silicon, or doped (acceptor or donor) single crystal silicon. As an optional feature, the substrate can be doped so that the surface of the substrate has a higher level of dopants than the bulk of the substrate. Substrate 10 acts as the bottom electrode for the capacitor of the present invention. As a result, an additional layer for a bottom electrode is not needed. This is beneficial in ultra high density devices where conservation of space is at a premium.

Next, a buffer layer 12 is established over substrate 10, as shown in Fig. 1. Buffer layer 12 can be established by, for example, E-Beam evaporation. Layer 12 can also be established by sputtering, chemical vapor deposition, or Sol-Gel technique, for example. Buffer layer 12 preferably is comprised of a film having a relatively high dielectric constant. If the dielectric constant of the buffer layer is too low, the buffer layer will act as a second capacitor in series with the layer of ferroelectric material, infra, and cause the effective dielectric constant of the capacitor to be significantly decreased.

Buffer layer 12 should also be fabricated so that there is no interdiffusion, which results in the formation of a low dielectric constant layer, between buffer layer 12 and substrate 10 and/or the overlying layer of ferroelectric material. Accordingly, buffer layer 12 is preferably comprised of a material which has a high melting point (well above 550°C), low porosity, and high resistivity. A material with a high density is also preferred. In addition, buffer layer 12 should be compatible with standard IC fabrication techniques. ZrO_2, LaO_2, and TiO_2 are examples of materials which meet these requirements for buffer layer 12. Preferably, buffer layer 12 is comprised of ZrO_2. Layer 12 has a thickness of approximately 300 Å (30 nm).

A layer of ferroelectric material 14 is then established on top of buffer layer 12. Layer 14 can be established by, for example, deposition. The deposition can be by sputtering from a composite oxide target, chemical vapor deposition, or Sol Gel technique, for example. The ferroelectric material in layer 14 preferably comprises a lead zirconate titanate composition, called "PZT", and having the general formula $Pb(Zr_xTi_{1-x})O_3$. The $Pb(Zr_xTi_{1-x})O_3$ stoichiometry can be in the range from X = 0 to X = 1.0. Layer 14 has a typical thickness of 3000 Å (300 nm). Of course, the thinner the dielectric layer, the greater the capacitance of the resulting capacitor, since capacitance is inversely proportional to the separation distance between the capacitor plates.

Layer 14 and buffer layer 12 are then patterned using standard photolithographic techniques and etched to form a stack having lateral edges which are co-linear. The etching can be done either in a wet HF solution, an ion mill, a plasma etch, or another anisotropic etch. The (stack) structure shown in Fig. 2 results.

The stack (of ferroelectric material 14 and buffer layer 12) is then annealed. Preferably, the stack is annealed at a temperature above 500°C in an O_2 ambient in order to convert the PZT into a high dielectric perovskite phase. Annealing can be done by either a rapid thermal anneal or furnace anneals.

A relatively conductive top electrode 16 is then established over layer 14. Top electrode 16 can be established by deposition, for example. The thickness of top electrode 16 is typically in the range between 1000 Å (100 nm) to 3000 Å (300 nm). Preferably, top electrode 16 is comprised of a noble metal. The noble metal can be, for example, platinum or palladium. In addition, the noble metal in top electrode 16 could be an alloy comprised of one of the following: platinum and palladium; platinum and titanium; platinum and bismuth; platinum and rhenium; platinum, palladium and titanium; platinum, bismuth and titanium; palladium and titanium; palladium and bismuth; palladium and rhenium; and palladium, bismuth and titanium. In another embodiment, top electrode 16 can be comprised of a doped polysilicon.

Top electrode 16 is then patterned using standard photolithographic techniques and etched by ion milling or plasma etching. Fig. 3 shows the resulting structure. The resulting capacitor has a dielectric constant at least 40 times that of a capacitor with a SiO_2 dielectric.

In a second embodiment shown in Fig. 4, a layer 11 of polysilicon is established over substrate 10. In this embodiment, layer 11 acts as the bottom electrode and individual access to the bottom electrode of the capacitor is possible. Typically, layer 11 has a thickness of 3000 Å (300 nm). Layers 12 and 14 are comprised of materials and established in a manner similar to the first embodiment. The stack comprising layers 11, 12 and 14 is then patterned, etched and annealed in a similar manner as in the first embodiment. Top electrode 15 is then established and patterned in a manner similar to that used in the first embodiment. Top electrode 16 is comprised of a noble metal.

Figure 5 shows a plan view of an embodiment of the structure of the present invention.

The capacitor of the present invention can be used in an array of capacitors or DRAMs. For example, the capacitors could be in an array having a common bottom electrode (i.e. the silicon substrate). The capacitor of the present invention can be utilized in an array by, for example, simply interconnecting the capacitors by extending the top electrode from one capacitor to the next. If individual access to the bottom electrode of each capacitor in the array is desired, the structure of the second embodiment of the present invention, wherein a layer of polysilicon 11 acts as the bottom electrode, can be used.

The structure of the present invention can also be used in a variety of devices requiring charge storage such as SRAM and ASIC designs.

This description has been offered for illustrative purposes only and is not intended to limit the invention of this application, which is defined in the claims below.

Claims

1. A semiconductor capacitor structure characterized by a substrate (10), a buffer layer (12) located over said substrate (10), a layer of ferroelectric material (14), located over said buffer layer (12) and a top electrode (16) located over said layer of ferroelectric material (12).

2. The capacitor of Claim 1 further characterized by said ferroelectric material being $Pb(Zr_xTi_{1-x})O_3$ wherein x is in the range of 0 to 1.0.

3. The capacitor of the preceding claims further characterized by said buffer layer being comprised of a material having a high dielectric constant.

4. The capacitor of the preceding claims further characterized by said buffer layer being comprised of a compound selected from the group comprised of zirconium oxide, lanthanum oxide and titanium oxide.

5. The capacitor of the preceding claims further characterized by said top electrode (16) being a noble metal which is an element selected from the group comprising platinum, palladium, titanium, bismuth, and rhenium.

6. The capacitor of Claims 2 , 3 and 4 further characterized by said top electrode (16) being comprised of polysilicon.

7. The capacitor of the preceding claims further characterized by said substrate being comprised of a material selected from the group comprising an undoped single crystal silicon, a doped (acceptor or donor) single crystal silicon layer and a polysilicon layer on a silicon substrate.

8. The capacitor of Claim 1 further characterized by a layer of polysilicon (11) being located over said substrate (10).

9. A method for fabricating a semiconductor capacitor structure, characterized by the steps of forming a substrate (10), establishing a buffer layer (12) over said substrate (10), establishing a layer of ferroelectric material (14) over said buffer layer (12), defining said buffer layer (12) and said layer of ferroelectric material (14) and establishing a top electrode (16) over said layer of ferroelectric material.

10. The method of Claim 9 further characterized by said buffer layer (12) and said layer of ferroelectric material (14) being patterned and etched simultaneously so that each layer's lateral edges are coincident.

11. The method of Claims 9 and 10 further characterized by including the step of annealing said buffer layer (12) and said layer of ferroelectric material (14), in an oxygen ambient at a temperature greater than 500 °C, before establishing said top electrode (16).

12. The method of Claims 9 - 11 further characterized by the step of establishing a layer of polysilicon (11) over said substrate (12).

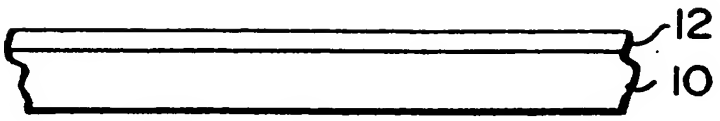

FIG. 1

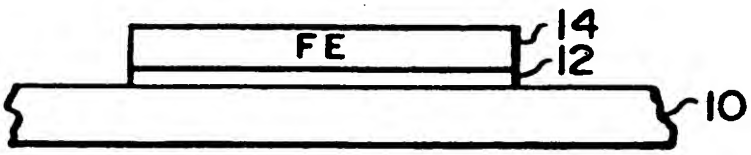

FIG. 2

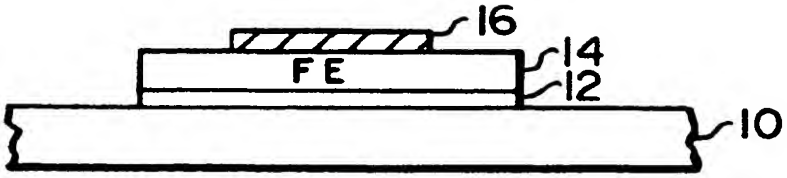

FIG. 3

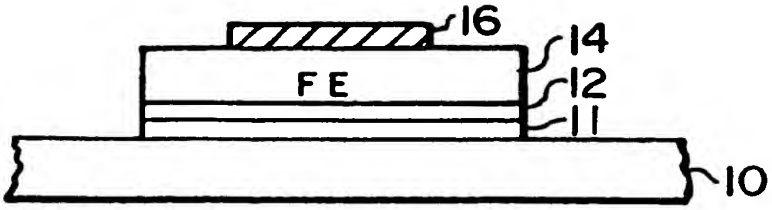

FIG. 4

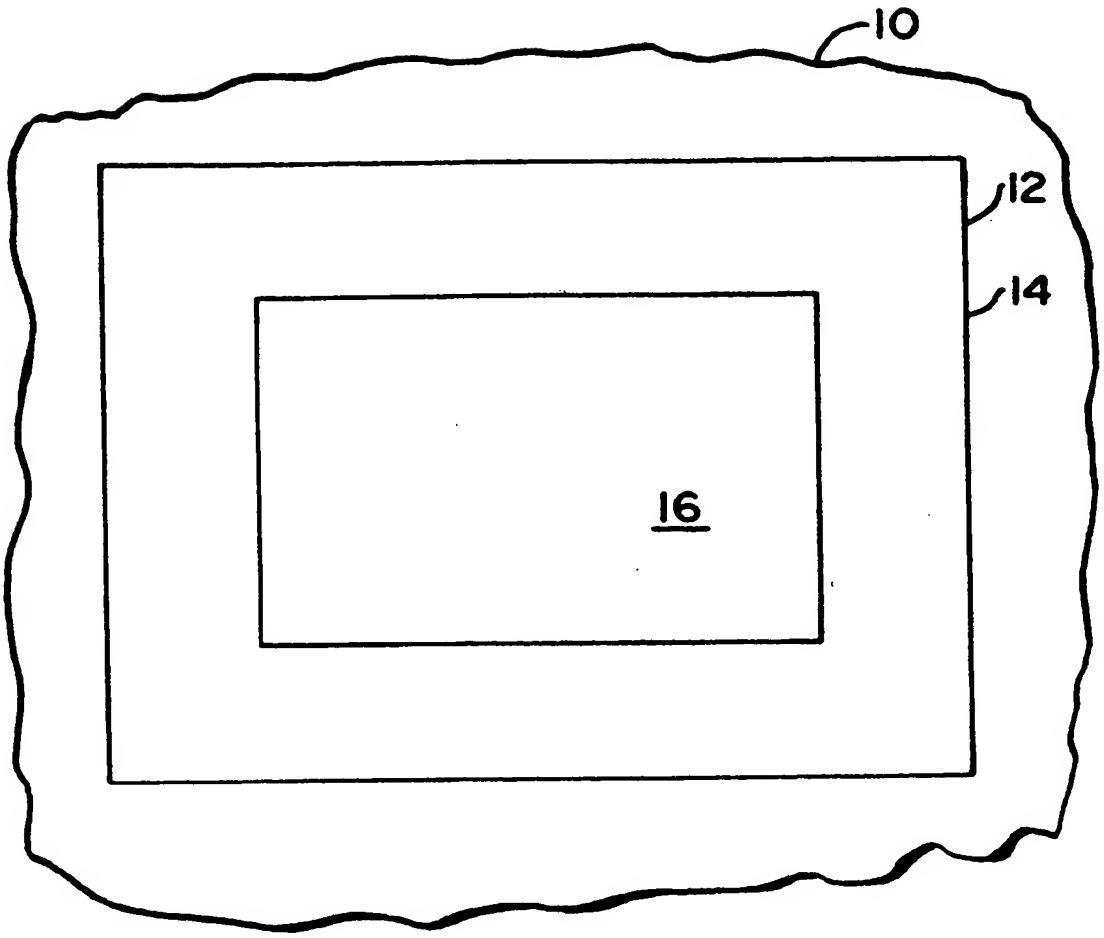

FIG.5

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EUROPEAN SEARCH REPORT

Application Number
EP 92 11 8382

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 415 750 (NEC CORP) 6 March 1991 * page 2, line 14 - page 2, line 55 * * page 5, line 57 - page 2, line 34; claims 1-9; figure 5 *	1,7-9, 11-12	H01L27/115 H01L29/94
A	JOURNAL OF APPLIED PHYSICS vol. 64, no. 5, 1 September 1988, NEW YORK US pages 2717 - 2724 GUANGHUA YI ET AL. 'Preparation of Pb(Zr,Ti)O3 thin films by sol gel processing: Electrical, optical, and electro-optic properties' * page 2718, right column - page 2718, left column *	1-4	
A	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 23, no. 12, May 1981, NEW YORK US pages 5373 - 5374 J.K. HOWARD 'Capacitor structure for bipolar memory device' * the whole document *	1,5,7-8	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24 FEBRUARY 1993	FRANSEN L.J.L.

CATEGORY OF CITED DOCUMENTS

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